FIG. 1
(PRIOR ART)

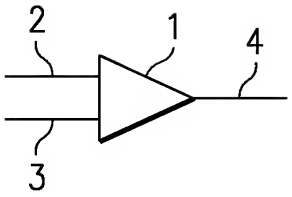


FIG. 2
(PRIOR ART)

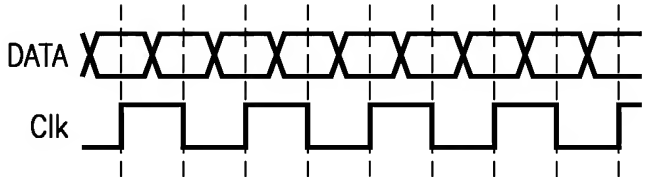


FIG. 3
(PRIOR ART)

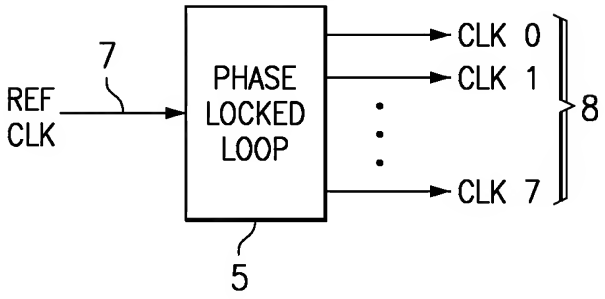


FIG. 4
(PRIOR ART)

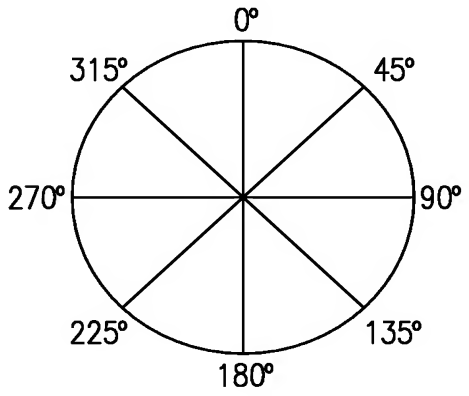


FIG. 5
(PRIOR ART)

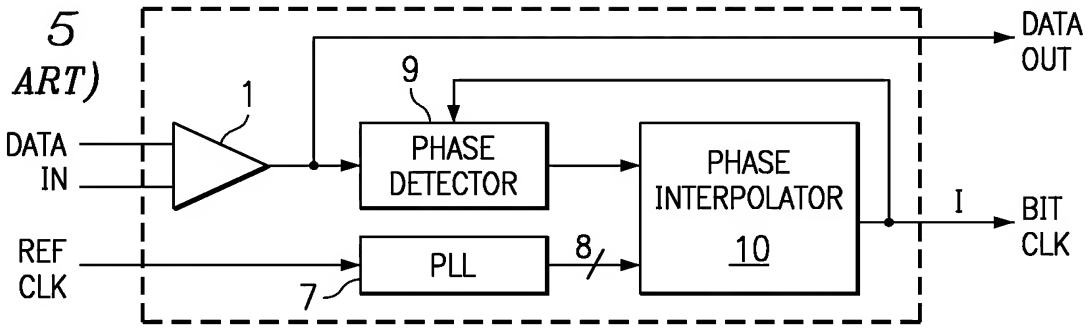
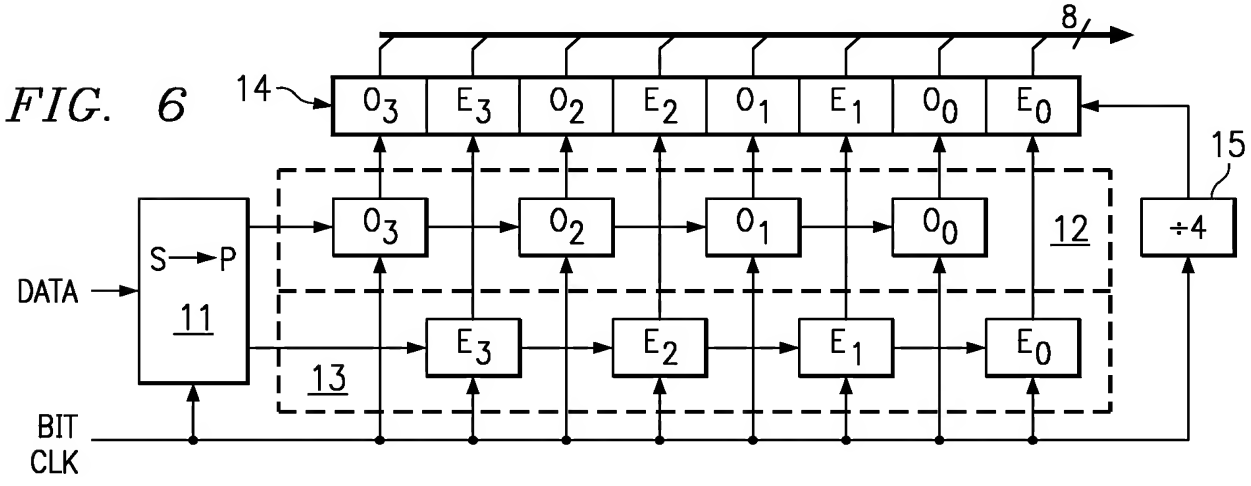


FIG. 6



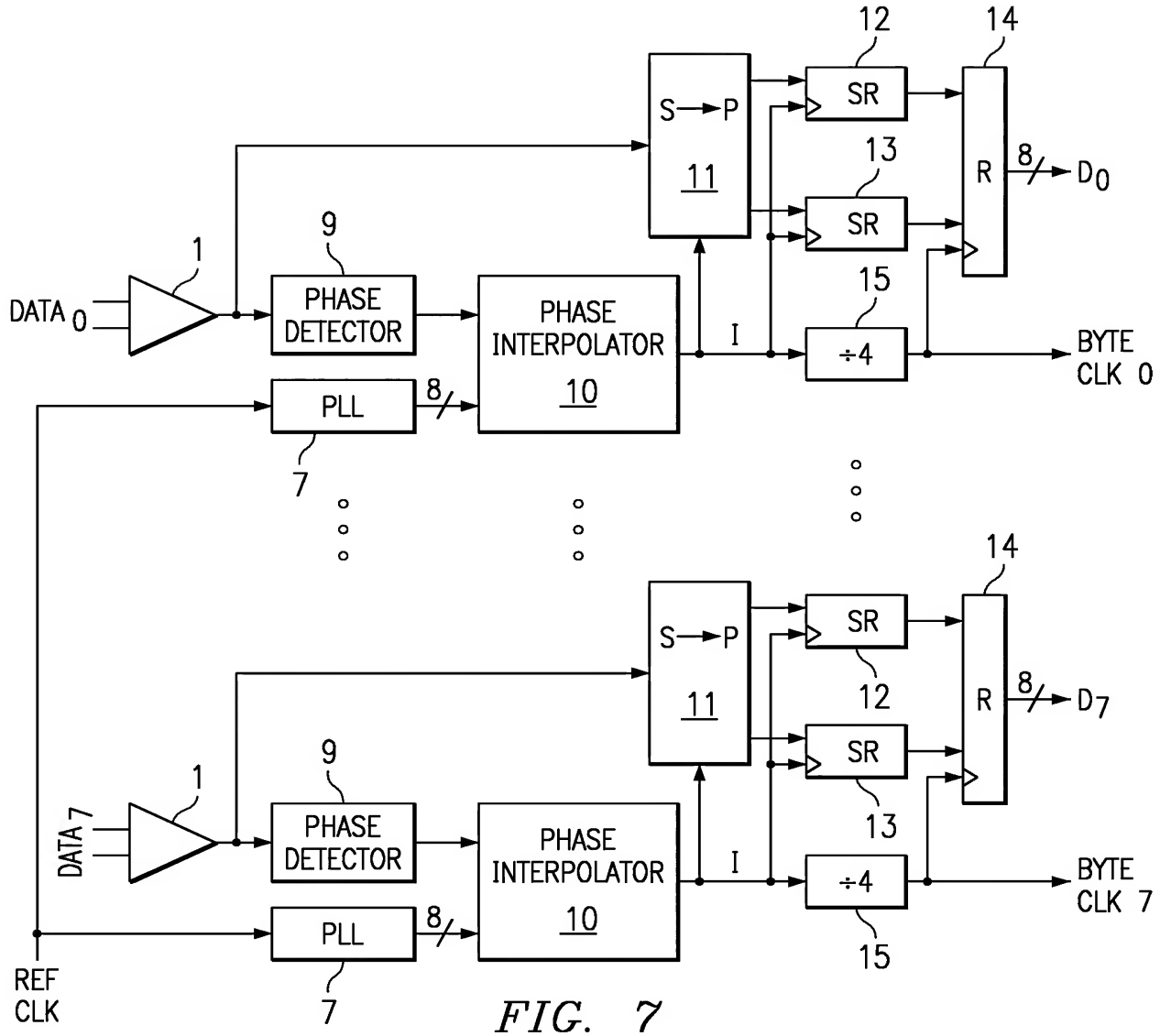

DATA 0
DATA 7
REF CLK
1
9
PHASE DETECTOR
PLL
8
7
PHASE INTERPOLATOR
10
I
S→P
11
12
13
14
15
SR
R
÷4
8
D0
D7
BYTE CLK 0
BYTE CLK 7

FIG. 7

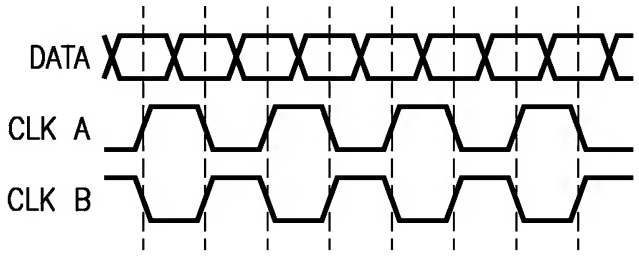

DATA
CLK A
CLK B

FIG. 8

FIG. 9

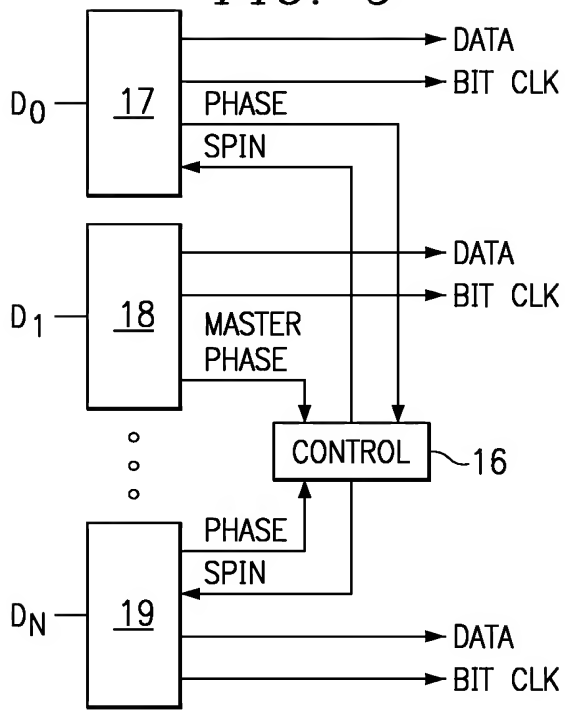


FIG. 10

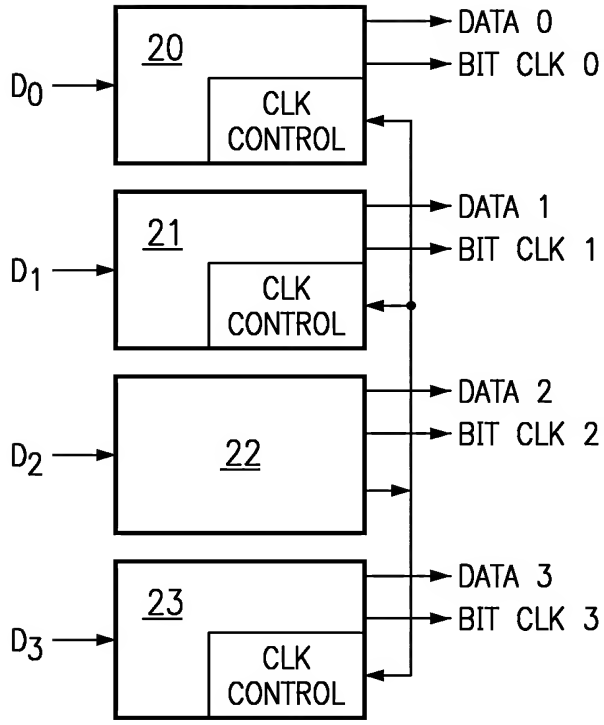
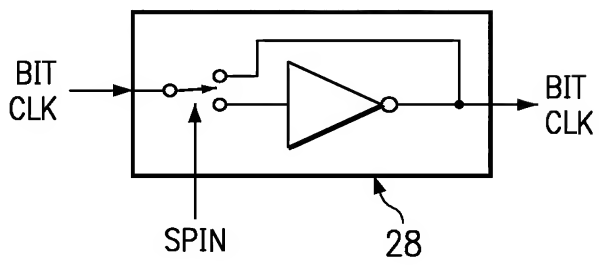


FIG. 9a



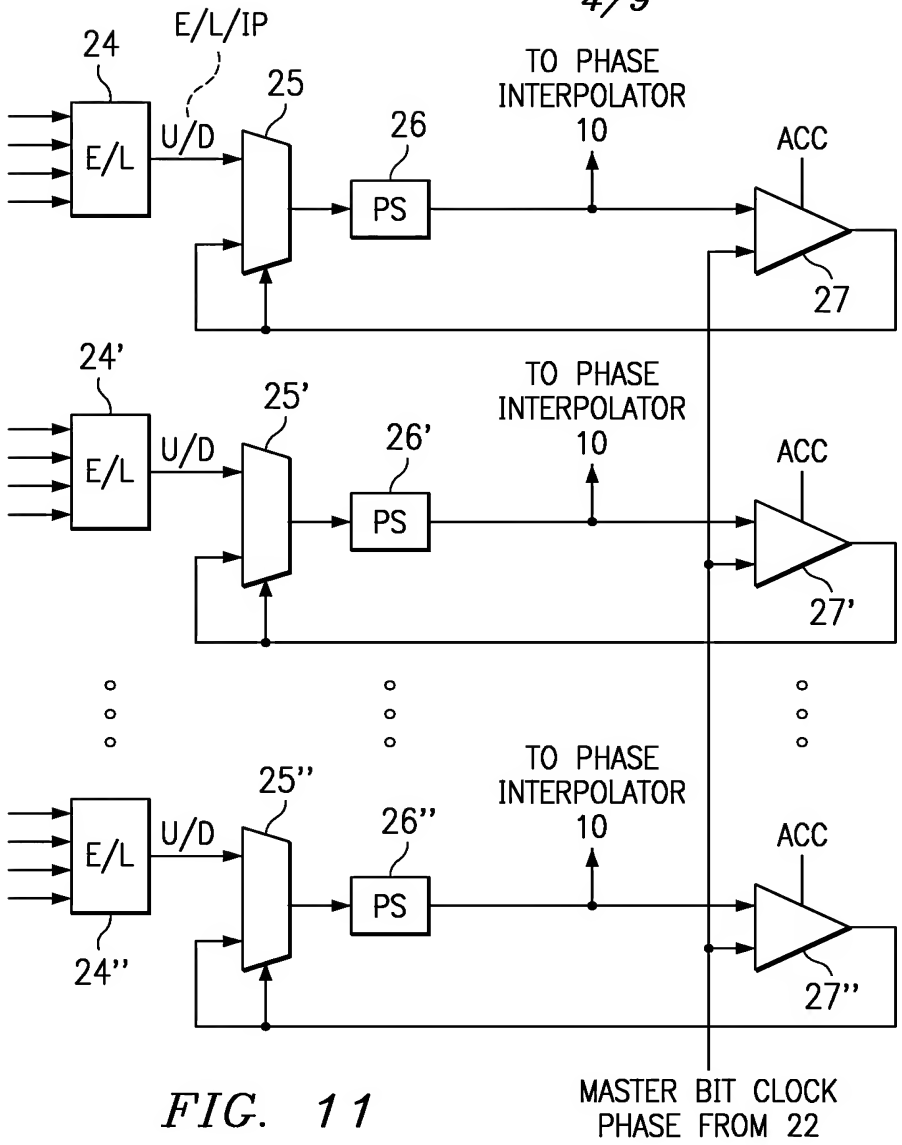


FIG. 11

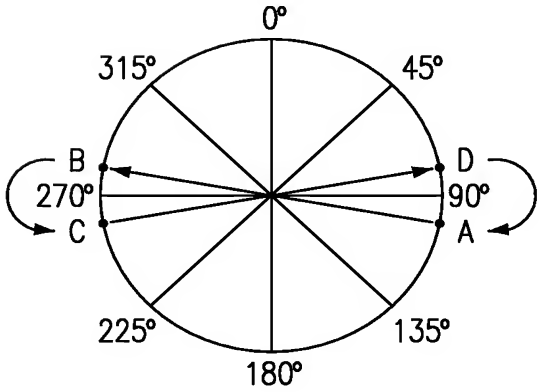


FIG. 12

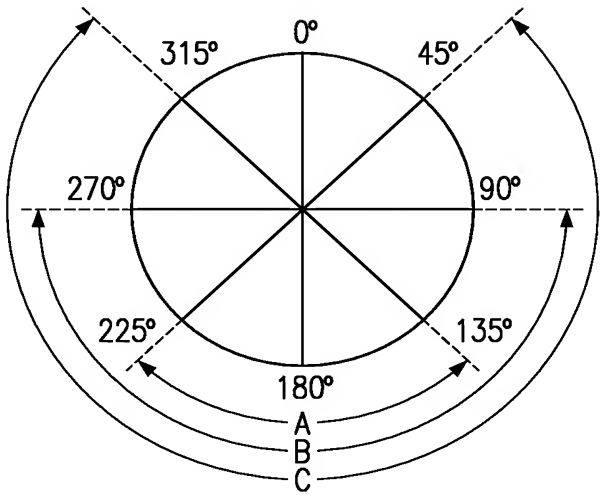


FIG. 13

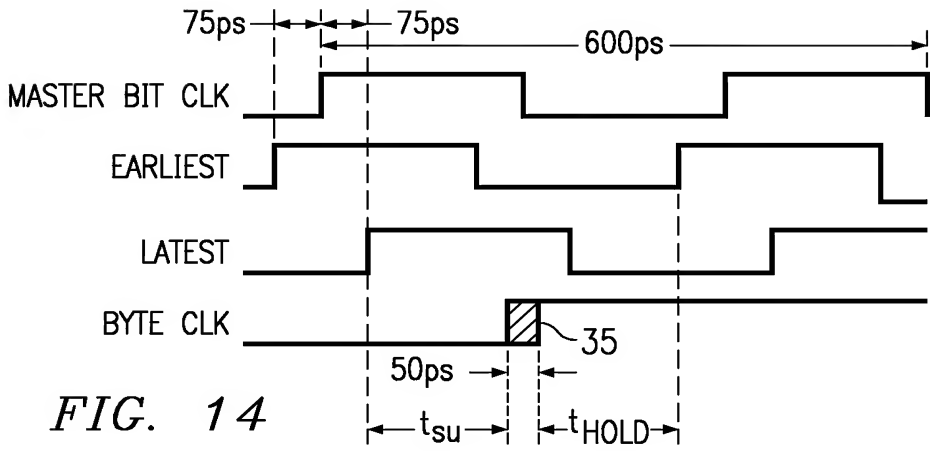


FIG. 14

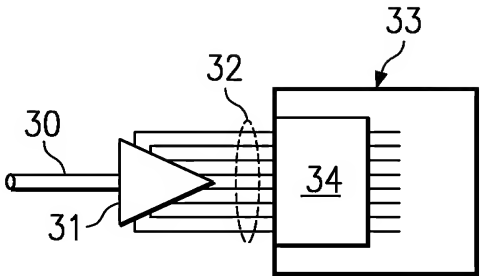


FIG. 15

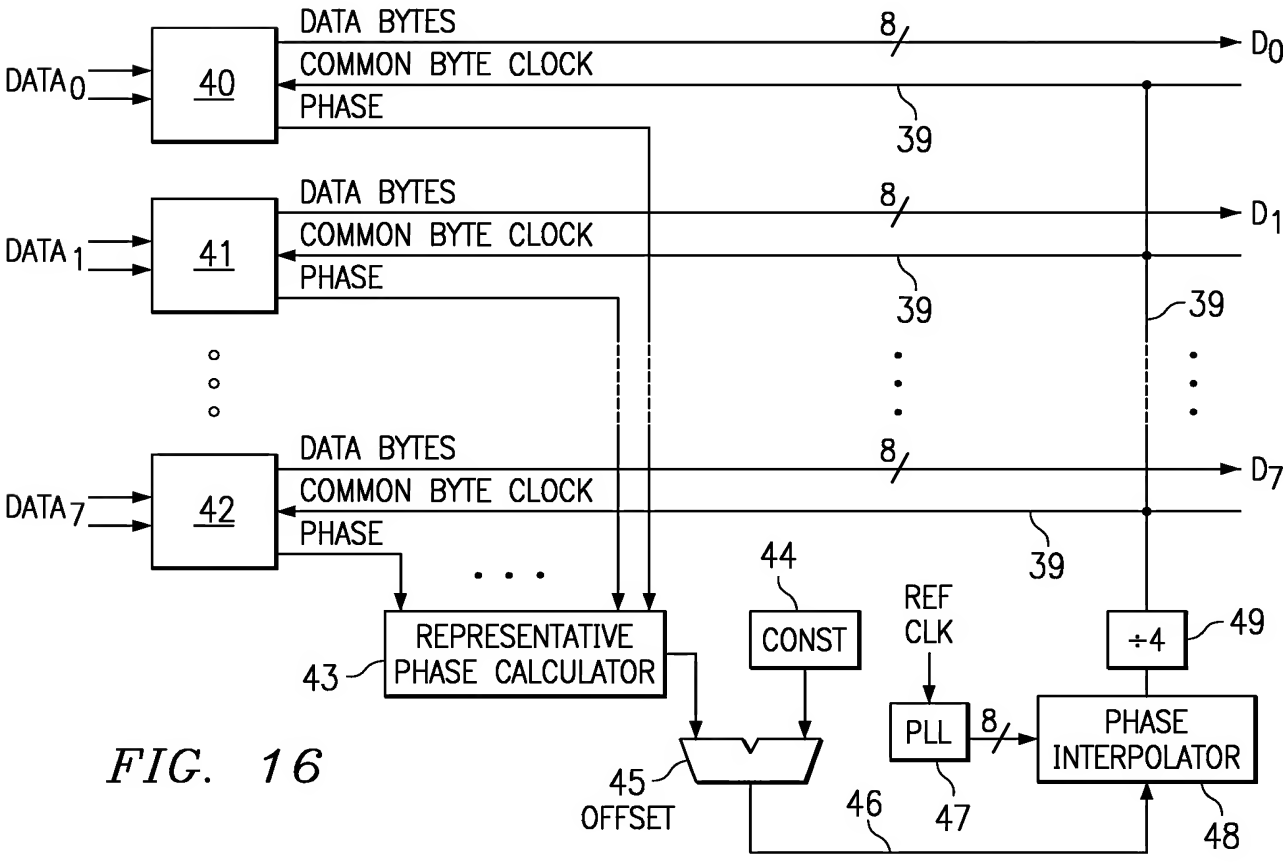


FIG. 16

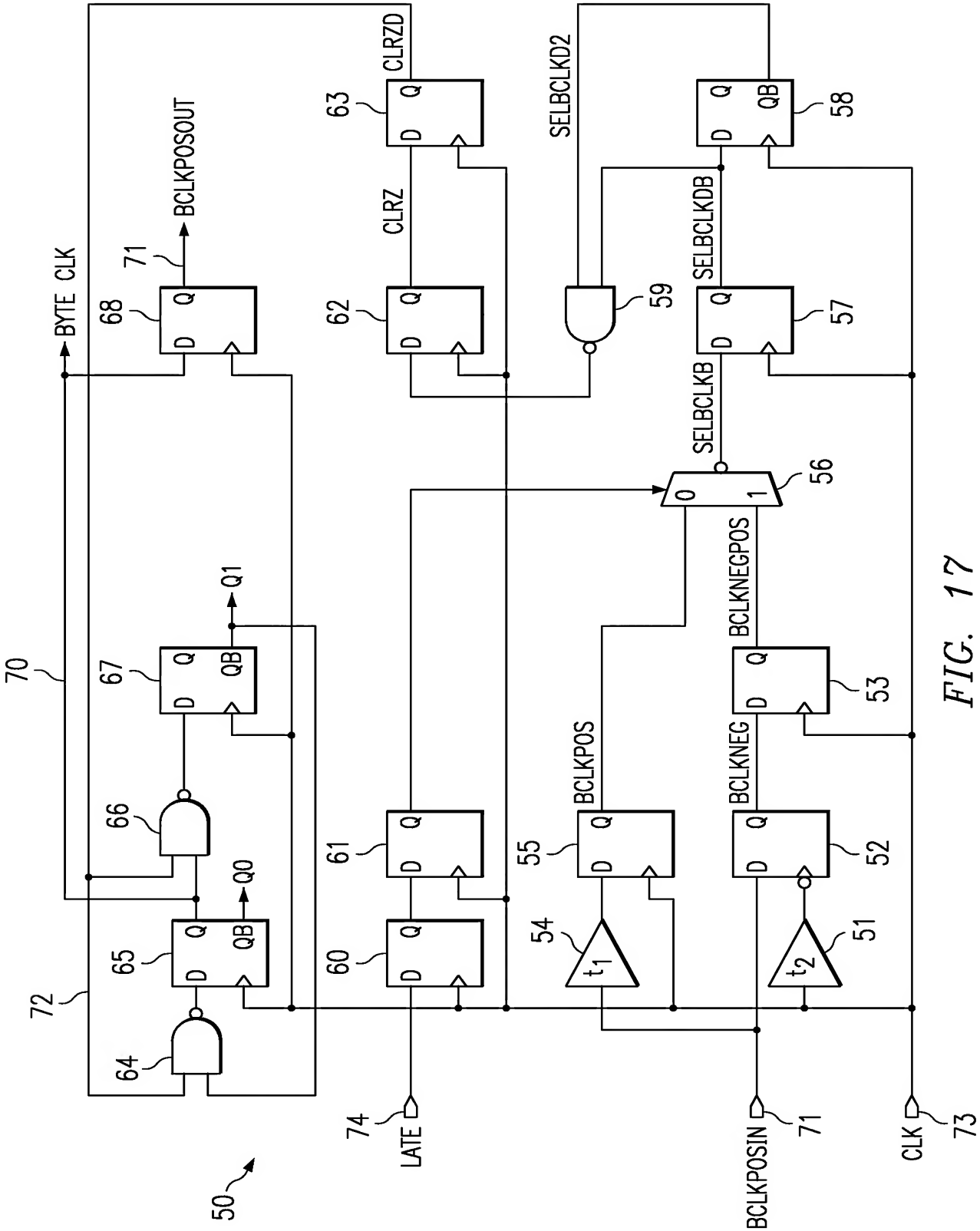

BYTE CLK
BCLKPOSOUT
71
68
CLRZD
63
CLRZ
62
SELBCLKD2
59
58
SELBCLKDB
57
SELBCLKB
56
Q1
67
70
66
Q0
65
72
64
61
60
BCLKPOS
55
54
t_1
BCLKNEGPOS
53
BCLKNEG
52
51
t_2
74
LATE
BCLKPOSIN
71
CLK
73
50

FIG. 17

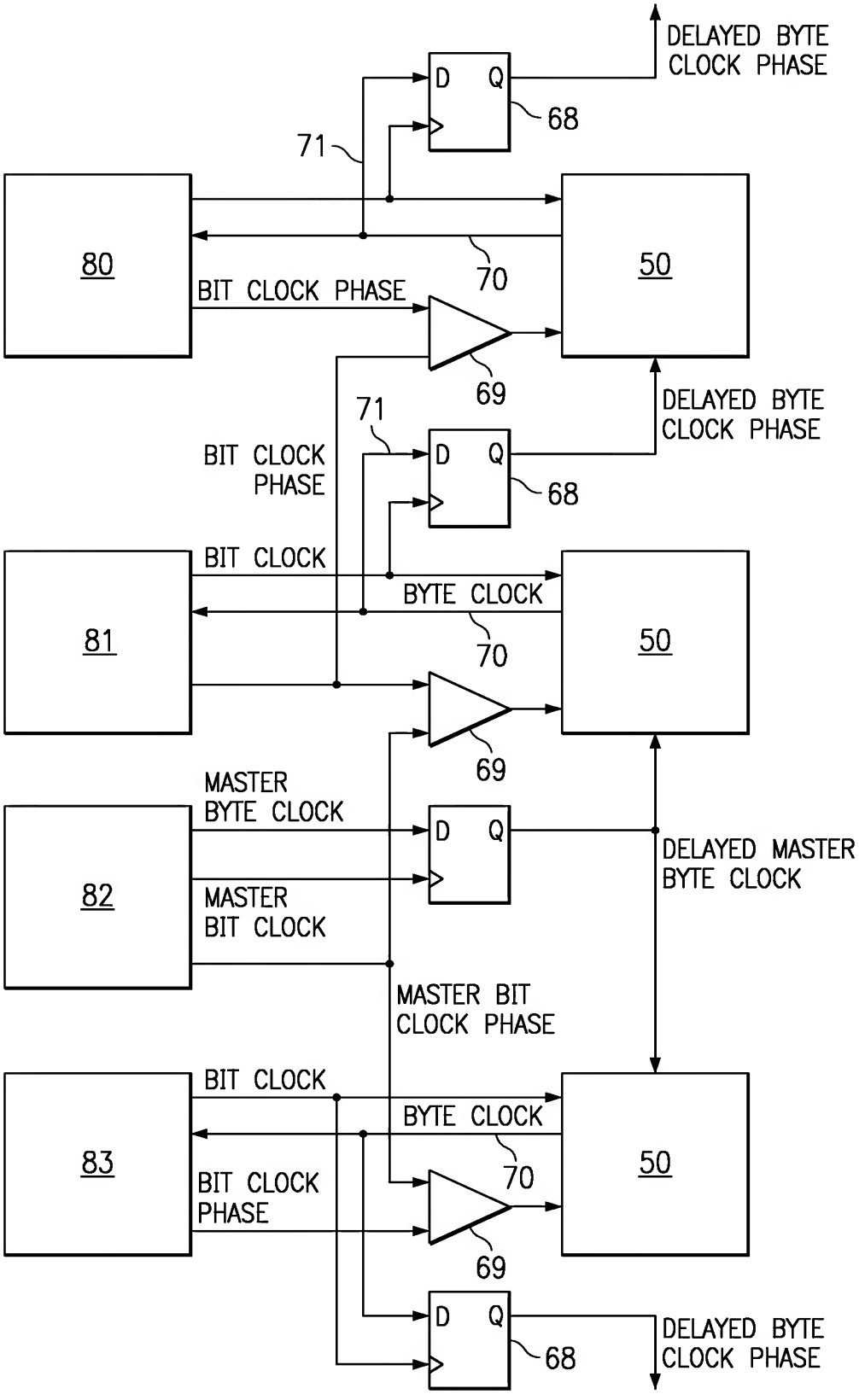
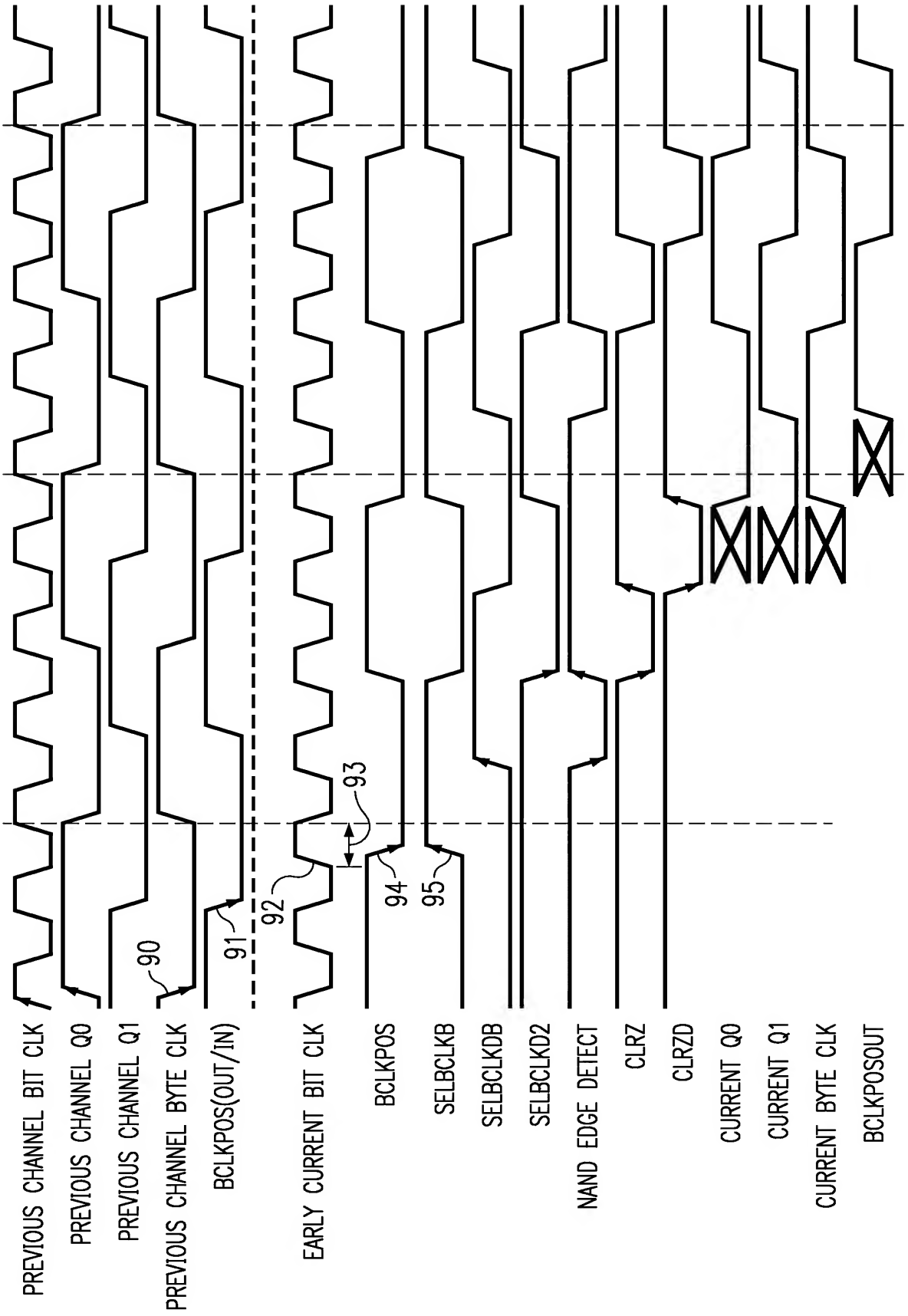

DELAYED BYTE
CLOCK PHASE
D
Q
68
71
80
70
50
BIT CLOCK PHASE
69
DELAYED BYTE
CLOCK PHASE
71
BIT CLOCK
PHASE
D
Q
68
BIT CLOCK
BYTE CLOCK
81
70
50
69
MASTER
BYTE CLOCK
D
Q
DELAYED MASTER
BYTE CLOCK
82
MASTER
BIT CLOCK
MASTER BIT
CLOCK PHASE
BIT CLOCK
BYTE CLOCK
83
70
50
BIT CLOCK
PHASE
69
D
Q
DELAYED BYTE
CLOCK PHASE
68

FIG. 18

FIG. 19


PREVIOUS CHANNEL BIT CLK
PREVIOUS CHANNEL Q0
PREVIOUS CHANNEL Q1
PREVIOUS CHANNEL BYTE CLK
BCLKPOS(OUT/IN)
EARLY CURRENT BIT CLK
BCLKPOS
SELBCLKB
SELBCLKDB
SELBCLKD2
NAND EDGE DETECT
CLRZ
CLRZD
CURRENT Q0
CURRENT Q1
CURRENT BYTE CLK
BCLKPOSOUT
90
91
92
93
94
95

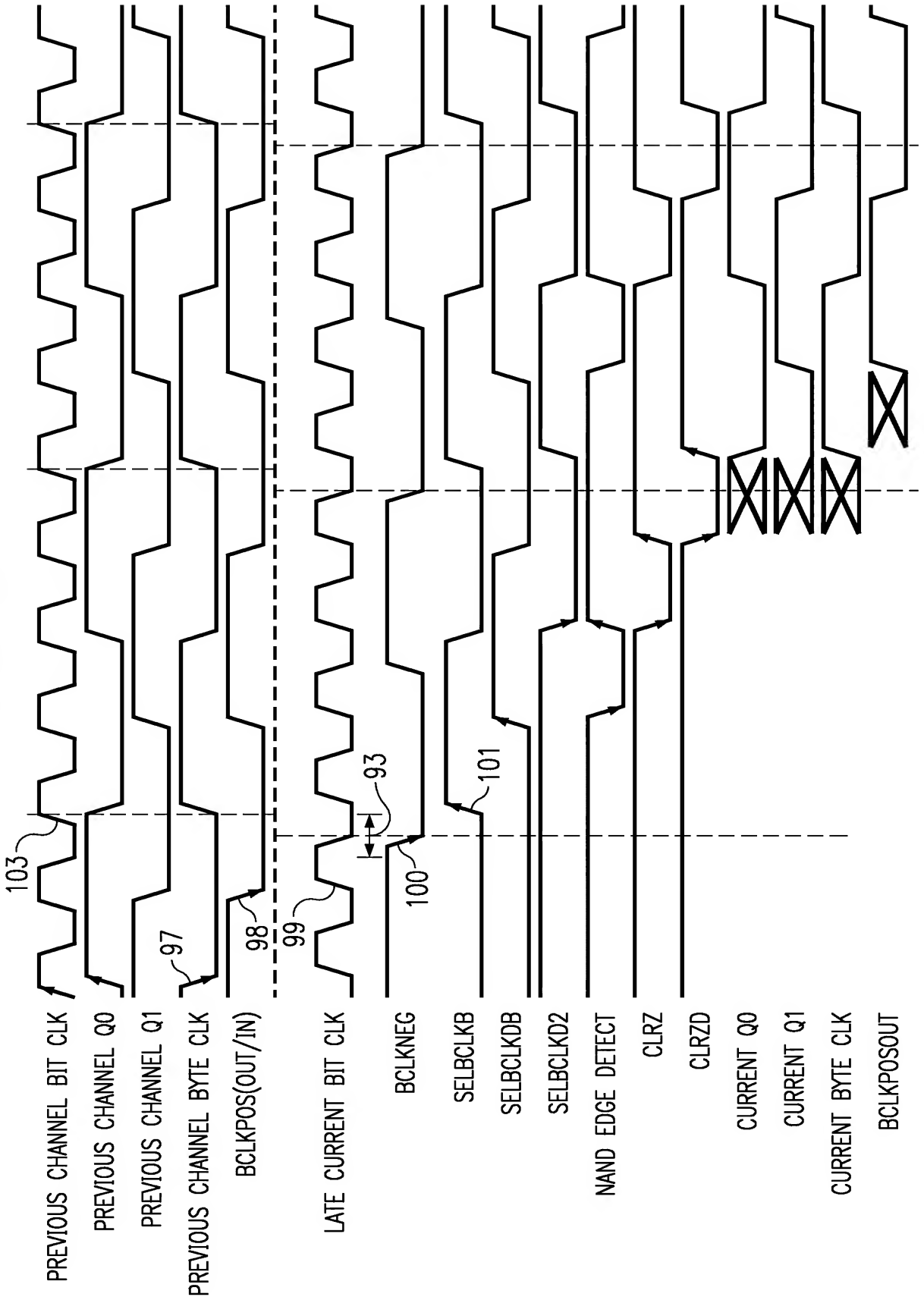

PREVIOUS CHANNEL BIT CLK
PREVIOUS CHANNEL Q0
PREVIOUS CHANNEL Q1
PREVIOUS CHANNEL BYTE CLK
BCLKPOS(OUT/IN)
LATE CURRENT BIT CLK
BCLKNEG
SELBCLKB
SELBCLKDB
SELBCLKD2
NAND EDGE DETECT
CLRZ
CLRZD
CURRENT Q0
CURRENT Q1
CURRENT BYTE CLK
BCLKPOSOUT
103
97
98
99
100
101
93

FIG. 20